METHOD OF GENERATING A SWITCHING SEQUENCE FOR AN UNARY ARRAY OF CONDUCTING BRANCHES AND A RELATIVE THERMOMETRICALLY DECODED DIGITAL-TO-ANALOG CONVERTER

PRIORITY CLAIM

[1] This application claims priority from European Patent Application No. 03425218.9 filed on April 7, 2003, which is incorporated herein by reference.

FIELD OF THE INVENTION

[2] An embodiment of the present invention relates generally to digital-analog converters and in particular to a method of generating a switching sequence for an unary array of conducting branches and a relative thermometrically decoded digital-to-analog converter having a desired integral non-linearity (briefly INL) error function.

BACKGROUND OF THE INVENTION

[3] Digital-analog (D/A) converters are widely used in many applications, such as wireless communications, signal reconstruction, waveforms generation etc. Basically, a D/A converter may be realized with an array of conducting branches that generate binary weighted constant currents (binary array) and/or identical currents (unary array). These conducting branches may include capacitors or current generators, selectable by respective switches for delivering current toward a summing line or toward ground.

[4] For sake of simplicity, let us refer to a D/A converter, the conducting branches of which are realized with current generators, though what will be said will hold, *mutatis mutandis*, also for conducting branches realized with switched capacitors.

[5] The conducting branches of a binary array are selected by respective bits of an input bit string, while the conducting branches of an unary array are selected according to a fixed switching sequence for making the unary array generate a total current corresponding to the input digital value.

[6] For better comprehending the field of utility of an embodiment of this invention, let us refer to the so-called segmented converters, which generally have a

binary weighted array of conducting branches, selected by the least significant bits of an input digital string, and an unary array that delivers a current corresponding to the digital value represented by the most significant bits, that is according to a so-called thermometer or thermometric decoding.

[7] A sample unary array is depicted in **FIG. 1**. As may be noticed, the current generators are selected according to a certain switching sequence and the output current ***Iout*** corresponds to the sum of the currents circulating in the selected branches. Optionally, there may be a "dummy" area in the unary array, which may be used for realizing biasing circuits. In segmented digital-to-analog converters, the "dummy" area may be used for realizing a binary array.

[8] When the digital input value to be converted by the unary array represents a certain number *n*, the current generators of the unary array from 1 to *n* are switched on, thus generating an output current ***Iout*** proportional to the digital input number *n*.

[9] Ideally, a D/A converter should generate an output signal that varies linearly with the input bit string, which would happen if all the conducting branches were identical. Unfortunately, mismatches between conducting branches due to inaccuracies of the fabrication process (process spread), make the current delivered by each branch not exactly equal to the design value, but affected by an error that may depend on the position of the conducting branch on the silicon substrate.

[10] In general, unary arrays are affected by a differential non-linearity (DNL) error and by an integral non-linearity (INL) error.

[11] Indicating with $\bar{I}$ the average current delivered by the branches of an unary array and with I_j the current delivered by the *j*-th branch of the array in the switching sequence,

$$I_j = \bar{I} \cdot (1 + \varepsilon_j)$$

wherein ε_j is the relative deviation of the current I_j from the average current $\bar{I}$.

[12] In an unary array not having a dummy area, the DNL error of the *k*-th branch in the switching sequence is

$$DNL(k) = \varepsilon_k$$

which represents a non-uniform deviation in the ideal current step amplitude between adjacent bit strings.

[13] The INL error function is defined as

$$INL(k) = \sum_{j=1}^{k} \varepsilon_j$$

and gives the deviation of the real analog output signal from its ideal value as a percentage of the average current $\bar{I}$ for any value "*k*" of the switching sequence.

[14] The absolute INL error of a switching sequence is the maximum absolute value of the relative INL error function.

[15] An introduction on the INL and DNL errors of an unary array of a D/A thermometrically decoded converter is carried out in the article by Y. Cong and R. L. Geiger "Switching Sequence Optimization for Gradient Error Compensation in Thermometer-Decoded DAC Arrays", *IEEE Trans. on circuits and systems - II: analog and digital signal processing*, Vol. 47, No. 7, pages 585-595, July 2000.

[16] The DNL error of a branch can be reduced only by reducing the process spread and is independent from the switching sequence. By contrast, the INL error function strongly depends on the switching sequence, as it may be easily inferred from the following example.

[17] Two possible switching sequences of a mono-dimensional unary array having eight conducting branches are shown in **FIG. 1A**. The conducting branches are affected by the indicated DNL errors (ε). The absolute values of the underlined numbers are the absolute INL errors of the switching sequences.

[18] As may be noticed, the INL error function of the sequential switching sequence shows a maximum deviation of the analog output from its ideal value in the middle of the sequence. This situation is inconvenient, because the digital values input to a D/A converter are more likely in the middle of the range of conversion, rather than at the two ends thereof. Therefore, it is more convenient to switch the mono-dimensional array of conducting branches of **FIG. 1A** according to a

symmetrical sequence than according to a sequential sequence. Moreover, the absolute INL error for the symmetrical sequence is ***7***, while for the sequential sequence is ***16***.

[19] In this very simple case, it is possible to determine by successive trials the switching sequence with the smallest absolute INL error, but for two-dimensional unary arrays of approximately one thousand conducting branches, the number of combinations is too large for determining a switching sequence with the desired INL error function by trials.

[20] Many different methods of determining a switching sequence of a two-dimensional unary array of conducting branches and a relative D/A converter have been proposed.

[21] The patent US 6,118,398 by G.J. Fisher et al. discloses a digital-analog converter having an unary array of current sources that are selected according to a sequence that ensures a relatively small absolute integral non-linearity error. The suggested switching sequence is substantially a mixed symmetrical sequence, in which the current sources that are in the middle of the array have median positions in the switching sequence, while current sources that are in borderline regions of the array are at the beginning or at the end of the sequence.

[22] The patent US 5,057,838 by K. Tsuji et al. discloses a D/A converter having a plurality of conducting branches of a two-dimensional array, wherein the switching sequence is determined in order to make the center of the current contributions delivered by the conducting branches of the array coincide with the center of the array.

[23] The document "A 14-bit Intrinsic Accuracy Q2 Random Walk CMOS DAC" by Van der Plas, Steyaert et al., JSCC 12 Dec '99, discloses a method of determining the switching sequence of the switches of a D/A converter organized in matrix form, exploiting the so-called "Q^2 random walk" algorithm.

[24] The document "Switching Sequence Optimization for Gradient Error Compensation in Thermometer-Decoded DAC Arrays", by Cong, Geiger, JSSC 7 Jul '00, discloses an algorithm to find the so-called "INL bounded" switching sequence for an unary array of branches organized in matrix form.

[25] Unfortunately, the absolute INL errors of the D/A converters realized with the above techniques remain relatively large.

SUMMARY OF THE INVENTION

[26] As will be more clearly described hereinafter, the array of conducting branches is affected by an error whose spatial distribution has an anti-symmetrical linear component, a quadratic symmetrical component, components of higher orders and a random component. The known thermometrically decoded converters are affected by quite large INL errors because the switching sequence of their unary array of conducting branches is not determined in a way that would optimally compensate the quadratic component of the error distribution.

[27] An embodiment of a method according to the invention determines switching sequences of two-dimensional unary arrays of conducting branches of thermometrically decoded D/A converters, in a way that will ensure that the relative INL error function is contained between pre-established symmetrical upper and lower bound functions. These functions may be constant, such to ensure an absolute INL error smaller than a pre-established value, or approaching zero in correspondence of midway values of the switching sequence from a certain maximum value in correspondence of the two ends of the range of conversion. This last solution is preferable when the D/A converter is likely to work almost constantly about the middle of its range of conversion.

[28] When these upper and lower bound functions are constant, the obtained switching sequence compensates both the linear and the quadratic component of the error distribution and therefore is affected by a very small absolute INL error, which depends essentially on the random component of the error distribution.

[29] An embodiment of a method according to the invention may be easily implemented by a computer program and allows the realization of thermometrically decoded D/A converters affected by a known limited INL error function.

BRIEF DESCRIPTION OF THE DRAWINGS

[30] The advantages of embodiments of this invention will become more evident through a detailed description referring to the attached drawings, wherein:

FIG. 1 illustrates a sample prior-art 16x16 unary array;

FIG. 1A compares the INL error functions of two switching sequences for a prior-art mono-dimensional array;

FIG. 2 shows a sample joint error distribution;

FIG. 3 shows how to build a switching sequence according to an embodiment of the method of this invention;

FIG. 4 shows a flow chart of a preferred embodiment of the method of this invention;

FIG. 5 depicts a switching sequence determined by using an embodiment of the method of this invention for a 16x16 unary array;

FIG. 6 depicts a sequential switching sequence for a 16x16 unary array according to a prior art method;

FIG. 7 depicts a symmetrical switching sequence for a 16x16 unary array according to a prior art method;

FIG. 8 depicts a switching sequence for a 16x16 unary array of the 12-bit thermometrically decoded D/A converter embedded in the commercial devices MTC-xx154, MTC-xx174 and MTC-xx454 of Alcatel Microelectronics according to a prior art method;

FIG. 9 depicts a switching sequence for a 16x16 unary array determined with a Q^2 random walk algorithm according to a prior art method;

FIG. 10 depicts an "INL bounded" switching sequence for a 16x16 unary array according to a prior art method;

FIG. 11 depicts a random switching sequence for a 16x16 unary array according to a prior art method;

FIG. 12 depicts an anti-symmetrical switching sequence in respect to the center of a 16x16 unary array according to a prior art method;

FIG. 13 depicts an improved anti-symmetrical switching sequence in respect to the center of a 16x16 unary array according to a prior art method;

FIGS. 14 and 15 compare the INL error functions of the switching sequences of Figures from 5 to 13 in function of the direction θ of the linear error distribution;

FIGS. 16 and 17 compare the maximum values of the absolute INL errors of many switching sequences obtained with known methods and an embodiment of the method of the invention for different values of the linear g_l and quadratic g_q coefficients; and

FIG. 18 depicts the switching sequence of an unary array of 1024 conducting branches of a 14-bit D/A converter of an embodiment of this invention, ten of which are thermometrically decoded.

DETAILED DESCRIPTION

[31] Before illustrating a method according to an embodiment of this invention, it is necessary to make some mathematical considerations.

[32] As stated hereinbefore, the conducting branches of an array are affected by an error, which in electronic equipment may be due to thermal and/or mechanical phenomena, doping differences, and other process spread mechanisms of inaccuracy, distributed according to an error distribution function over the array.

[33] In general, for a two-dimensional disposition of conducting branches, the relative error distribution $\varepsilon(x,y)$ may be approximated by a Taylor series expansion:

$$\varepsilon(x,y) = a_0 + a_{11}x + a_{12}y + a_{21}x^2 + a_{22}y^2 + a_{23}xy + \cdots$$

[34] Truncating this series at the second order, neglecting the term $a_{23}xy$ and supposing that a_{21}=a_{22}, the linear $\varepsilon_l(x,y)$, quadratic $\varepsilon_q(x,y)$ and joint $\varepsilon_j(x,y)$ error distribution functions are, respectively,

$$\varepsilon_l(x,y) = g_l \cdot (\cos\theta \cdot x + \sin\theta \cdot y); \qquad \varepsilon_q(x,y) = g_q \cdot (x^2 + y^2) - a_0;$$

$$\varepsilon_j(x,y) = \varepsilon_l(x,y) + \varepsilon_q(x,y)$$

wherein θ is the angle of the linear error gradient, g_l is the slope, g_q is a quadratic coefficient and a_0 is an offset value. This joint error distribution, represented in **FIG. 2**, has proven to be a good approximation of real error distribution functions of unary arrays. The difference between the real error distribution and the joint error distribution is due to the components of higher order thereof and to a random error component.

[35] In order to compensate errors due to the linear component of the error distribution, according to an embodiment of a method of the invention, each pair of consecutive odd (2n-1) and even (2n) components of the switching sequence must be symmetrical in respect to the "center of gravity" of the two-dimensional array. In fact

$$\varepsilon_l(x,y) = -\varepsilon_l(-x,-y)$$

and thus, if pairs of consecutive branches {*a,b*} and {*g,h*} are disposed as depicted in **FIG. 3**, the linear component of the error introduced by each pair is null.

[36] Being that $\overline{\varepsilon_q}$ is the continuous component of the quadratic error distribution over the area of the array of branches, that is the mean value thereof, the quadratic error distribution is also given by

$$\varepsilon_q(x,y) = \overline{\varepsilon_q} + \varepsilon_q^{AC}(x,y)$$

wherein $\varepsilon_q^{AC}(x,y)$ is the alternate component of the quadratic error.

[37] The offset term $\overline{\varepsilon_q}$ does not contribute to the INL error because it causes only an offset error in the slope of the transfer function of the D/A converter. On the contrary, the alternate component has positive and negative values that make the transfer function nonlinear, thus originating the INL error.

[38] Therefore it is clear that, in order to have a switching sequence with a desired (small) INL error function, it is necessary to compensate for the alternate component of the quadratic error distribution.

[39] According to an essential embodiment of a method of an embodiment of the invention, the first step consists in defining an upper bound function and a lower bound function, symmetrical to each other, of the INL error function of the switching sequence to be generated. Then the error distribution function over the array is evaluated, in order to calculate the error associated to each pair of symmetrical branches. As stated before, each pair of successive branches must be symmetrical in respect to the center of gravity in order to compensate the component of the INL due to the linear error distribution.

[40] These bound functions define the range of variation of the INL error and they may be constant, if the absolute INL error must be minimized.

[41] The appropriate switching sequence is built by choosing a first pair of branches (1, 2) starting from any branch of the array and performing iteratively the following steps:

- calculating a corresponding value of the INL error function of the switching sequence being built,
- choosing as the successive pair, the pair of conducting branches that maximizes or minimizes the next value of the INL error function of the switching sequence though remaining comprised between the corresponding values of the upper bound and lower bound functions,
- if all other pairs do not meet the preceding conditions, then repeating the steps restarting from the first by choosing every time a different first pair of branches, and if the conditions cannot yet be met, changing at least one of the bound functions and restarting from the first step.

[42] Finally, when the determination of the appropriate switching sequence has been completed, it is output.

[43] Preferably, the above-described method is repeated for all possible first pairs of conducting branches, thus generating a set of switching sequences affected by an INL error function comprised between the same bound functions. The optimal switching sequence is chosen from this set according to a pre-established criterion.

[44] Optionally, the bound functions may be closer to zero in correspondence of midway values of the range of the converter compared to their value in correspondence of the two ends of the range of the converter.

[45] A preferred embodiment of a method of this invention is described by the flow chart of **FIG. 4**. In this case the symmetrical bound functions are constant and this constant value is half the maximum absolute value of the DNL error of the array.

[46] An example of a 16x16 matrix describing a switching sequence determined according to a method of an embodiment of the invention illustrated in **FIG. 4** and for $g_l = g_q = 0.5$ is depicted in **FIG. 5**. As may be noticed, the switching sequence has been determined by selecting every even conducting branch (2, 4, 6 ...) symmetrical to the preceding odd branch (1, 3, 5 ...) in respect to the center of the array.

[47] Preferably, but not necessarily, the map of the switching sequence will be anti-symmetrical in respect to an axis of symmetry of the array, that means that the last branch of the sequence is symmetrical to the first branch in respect to that axis of symmetry, and so forth for the other branches. For example, the positions of the branches 256, 255, 254, etc. of the switching sequence of **FIG. 5** are symmetrical to the positions of the branches 1, 2, 3, etc. in respect to the horizontal axis of symmetry of the array.

[48] For comparison purposes, eight other matrices obtained with different algorithms are depicted in **FIGS. 6 to 13**.

[49] The resulting absolute INL error values in function of the angle θ of the gradient of the linear error are compared in **FIGS. 14 and 15** for $g_l = g_q = 0.5$. The values have been calculated after having normalized to 1 the maximum value of the linear or quadratic errors. As may be noticed, the absolute INL error of the switching sequence of **FIG. 5** is always smaller than that of the other sequences.

[50] Moreover, differently from the switching sequences of **FIGS 6 to 13** obtained by using the known methods, the absolute INL error of the switching sequence of **FIG. 5** is substantially independent from the angle θ. This is very important because it ensures that the method of an embodiment of the invention is not tied to a particular shape of the error distribution, as is the method disclosed in the aforementioned paper by Y. Cong and R. L. Geiger.

[51] **FIG. 16** compares many switching sequences, indicating the maximum value of the absolute INL error for each of them. The references [1] and [2] indicate that the switching sequence is obtained using the method described in the above-mentioned papers by G. A. Van der Plas et al. and by Y. Cong and R. L. Geiger, respectively.

[52] As may be noticed, the switching sequence of Figure 5 is the best one. This result is confirmed even using different values of g_l and g_q, as shown in **FIG. 17**. Even if these parameters undergo sensible variations, the maximum absolute INL error of the switching sequence obtained with an embodiment of the present invention is substantially independent from them. This extraordinary result confirms that the method of an embodiment of this invention effectively compensates both the linear and the quadratic component of the error distribution.

[53] The method of an embodiment of this invention may be applied whichever the shape of the array of conducting branches is, not only to two-dimensional square arrays.

[54] A switching sequence generated according to a preferred embodiment of the method illustrated in **FIG. 4** for a substantially oval unary array of conducting branches of a 14-bit D/A converter of an embodiment of the invention, ten of which are thermometrically decoded, is depicted in **FIG. 18**. As may be noticed, the switching sequence is anti-symmetrical in respect to the vertical axis of symmetry. The ten most significant bits of the input bit string of the D/A converter of the invention are thermometrically decoded, while the four least significant bits select as many conducting branches of a binary scaled array.